What is claimed is:

1. A method for increasing the data throughput performance of a memory controller, comprising:

receiving data from a source;

compressing said data;

storing said data in memory;

reading said data from said memory;

decompressing said data; and

providing said data to a data consumer.

2. The method of Claim 1, wherein said data is received from said source at a first data rate.

3. The method of Claim 2, wherein said memory is capable of storing said data at a second data rate, wherein said first data rate is greater than said second data rate.

4. The method of Claim 3, wherein said data is provided to said destination at a third data rate, wherein said third data rage is greater than said second data rate.

5. The method of Claim 1, wherein said steps of compressing said data and decompressing said data are performed by an application specific integrated circuit (ASIC).

6. The method of Claim 1, wherein said steps of compressing said data and decompressing said data are performed by at least one of microcode and firmware running on a programmable microprocessor.

7. The method of Claim 5, wherein said memory is external to said application specific integrated circuit.

8. The method of Claim 5, wherein said memory is internal to said application specific integrated circuit.

9. The method of Claim 1, further comprising decompressing said compressed data from said memory to a temporary buffer in response to receiving a request for random access to said compressed data.

10. The method of Claim 1, further comprising:

receiving additional data;

determining whether said additional data is capable of compression; and

storing at least a portion of said additional data in said memory without first compressing said additional data if said data cannot be compressed.

11. The method of Claim 1, wherein said data source comprises at least one of a host system memory, a host processor, and a peripheral device.

12. The method of Claim 1, wherein said data consumer comprises at least one of a host system memory, a host processor, and a peripheral device.

13. The method of Claim 1, wherein said data is received from said source by at least one of a first interface and a second interface, and wherein said data is provided to said data consumer by at least one of said first interface and said second interface.

14. The method of Claim 1, wherein said data is received from said source by a first interface, and wherein said data is provided to said data consumer by a second interface.

15. A method for increasing disk drive controller data throughput, comprising:

receiving uncompressed first data at a first interface;

compressing said uncompressed first data to form compressed first data;

writing said compressed first data to memory;

reading said compressed first data from said memory;

uncompressing said compressed first data to recover said uncompressed first data; and

providing said uncompressed first data to at least one of said first interface and a second interface.

16. The method of Claim 15, wherein said first and second interfaces are capable of passing data at a first data rate, wherein said memory is capable of receiving data at a second data rate, and wherein said first data rate is greater than said second data rate.

17. The method of Claim 15, wherein said first interface is interconnected to a host system bus, and wherein said step of receiving uncompressed first data at said first interface comprises receiving uncompressed data from a data source comprising at least one of a host system memory, a host system processor interconnected to said host system bus, and a peripheral device.

18. The method of Claim 15, wherein said second interface comprises a channel of a storage device, and further comprising providing said uncompressed first data from said

second interface to said storage device.

19. The method of Claim 18, wherein said storage device comprises at least one of a hard disk drive, a tape drive, an optical drive, and a three-dimensional storage device.

20. The method of Claim 15, further comprising:

receiving uncompressed second data at said second interface;

compressing said uncompressed second data to form compressed second data;

writing said compressed second data to memory;

reading said compressed second data from memory;

uncompressing said compressed second data to recover said uncompressed second data; and

providing said uncompressed second data to at least one of said first interface and said second interface.

21. The method of Claim 15, wherein said step of compressing said uncompressed first data comprises compressing said uncompressed first data while said uncompressed first data is written to said memory.

22. The method of Claim 20, wherein said step of compressing said uncompressed second data comprises compressing said uncompressed second data while said uncompressed second data is written to said memory.

23. The method of Claim 15, further comprising:

receiving uncompressed second data at a first interface;

performing a compression routine with respect to at least a first portion of said second data, wherein said compression routine expands said second data;

writing at least a second portion of said second data to said memory without performing said compression routine with respect to said at least said second portion of said second data.

24. The method of Claim 15, wherein said second portion of said second data comprises substantially all of said second data.

25. The method of Claim 15, wherein said second portion comprises all of said second data.

26. The method of Claim 23, further comprising:

reading said second data from said memory;

decompressing said at least a second portion of said second data; and

providing said second data to at least one of said first interface and said second interface.

27. A memory controller, comprising:

a first interface having a first data bandwidth;

a second interface having a second data bandwidth;

data compression circuitry;

memory having a third data bandwidth; and

data decompression circuitry, wherein first data received at said first interface is compressed by said data compression circuitry for storage in said memory, and wherein said first data read from said memory is decompressed by said data decompression circuitry prior to being provided to at least one of said first interface and said second interface.

28. The memory controller of Claim 27, wherein said first data bandwidth plus said second data bandwidth is greater than said third data bandwidth.

29. The memory controller of Claim 27, wherein said data compression circuitry and said data decompression circuitry has a fourth data bandwidth, and wherein said fourth data bandwidth is greater than said third data bandwidth.

30. The memory controller of Claim 27, wherein at least one of said data compression circuitry and said data decompression circuitry comprise an application specific integrated circuit.

31. The memory controller of Claim 30, wherein said memory is external to said

application specific integrated circuit.

32. The memory controller of Claim 30, wherein said memory is internal to said application specific integrated circuit.

33. The memory controller of Claim 27, wherein said memory comprises at least one of RAM, DRAM, and SDRAM.

34. The memory controller of Claim 27, wherein said first interface is interconnected to a host computer.

35. The memory controller of Claim 27, wherein said second interface is interconnected to at least a first data storage device.

36. The memory controller of Claim 35, wherein said at least a first data storage device comprises a hard disk drive.

37. The memory controller of Claim 27, wherein said memory controller is implemented within a controller of a data storage device.

38. The memory controller of Claim 37, wherein said data storage device comprises a hard disk drive.

39. The memory controller of Claim 27, wherein at least a first portion of second data received at said first interface is expanded by said data compression circuitry, and wherein at least a second portion of said second data is stored in said memory in uncompressed form.

40. A method for providing a memory controller for a hard disk drive, comprising:

receiving first data at one of a first interface and a second interface;

compressing said first data;

after said step of compressing said first data, writing said compressed first data to memory;

reading said compressed first data from memory;

after said step of reading said first data, decompressing said compressed first data;

providing said uncompressed first data to at least one of said first interface and said second interface;

receiving second data at one of said first interface and said second interface;

compressing at least a first portion of said second data, wherein said step of compressing results in an expansion of said data;

after said step of compressing at least a first portion of said second data, writing at least a second portion of said second data to said memory without compressing said at least a second portion of said second data;

providing said at least a second portion of said second data to at least one of said first interface and said second interface.

41. The method of Claim 40, further comprising:

setting a first compression flag to signal that said first data has been compressed.

42. The method of Claim 40, wherein said second interface comprises a channel of a peripheral device.

43. The method of Claim 40, further comprising:

performing a CRC operation on said first data;

providing at least one of a parity value and an error correction code to said at least one of said first interface and said second interface.